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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/659,836

09/11/2003

Paul F.L. Weindorf

10541-1836

5526

29074

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07/19/2006

EXAMINER

BENENSON, BORIS

VISTEON

C/O BRINKS HOFER GILSON & LIONE

PO BOX 10395

CHICAGO, IL 60610

ART UNIT

PAPER NUMBER

2836

DATE MAILED: 07/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.		Applicant(s)	
	10/659,836		WEINDORF ET AL.	
	Examiner		Art Unit	
	Boris Benenson		2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 11 September 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-25 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☐ Claim(s) 1-4, 11-16 and 23-25 is/are rejected.
- 7) ☐ Claim(s) 5-10 and 17-22 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 11 September 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date <u>9/11/03, 11/22/04</u> | 6) <input type="checkbox"/> Other: _____ |

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Detailed Actions

Claim Objections

1. Claims 1 and 14 are objected to because of the following informalities:

Claims recite the limitation " a termination resistor I electrical connection with **the switch**". There is insufficient antecedent basis for this limitation in the claim. There is no consistency in terminology. In examiners opinion a terminology of the claims is not consistent. In examiners opinion the first transistor and the switch are different names for the same element. What elements described as the first transistor and the switch?

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the

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art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-4, 11, 14-16, and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawabata (JP2000338928) in view of Lee (5,716,323). Kawabata disclosed a circuit comprising a video input terminal (111) for receiving a video signal, a switch in electrical connected in series between the video input terminal and a termination resistor (107). Kawabata did not disclose a structure of the switch. Lee teaches a circuit where a propagation of a video input signal controlled by a switch (Fig. 3, Pos. S1). Lee teaches, "Switch S.sub.1 represents MOS/FET transistor Q.sub.1" (Col.5, Line 55). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified Kawabata with teachings of Lee and use MOSFET as a switch, because solid state MOSFET switch is known in the art and provide reliable and fast switching and because ordinary skill in the art would know how to connect and control NMOS or PMOS transistors.

Referring to Claims 2 and 16, the switch of Kawabata (the first transistor) limits voltage applied to the termination resistor.

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Referring to Claims 11 and 23, Kawabata disclosed a zener diode (101) connected between video input terminal (111) and ground terminal (112).

3. Claims 12-13 and 24-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawabata (JP2000338928) in view of Lee (5,716,323) as applied to claims 1 and 11 above, and further in view of Marum et al. (5,500,546). Kawabata disclosed a zener diode, but did not disclose "a second zener diode in electrical series connection with the first zener diode". Marum et al. teach an ESD Protection Circuits Using Zener Diodes, wherein two zener diodes connected back to back to each other (Figs. 3a, 3b). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified circuit of Kawabata in view of Lee with teachings of Lee and install two zener diodes back to back, because it will protect the circuit from a positive and a negative voltage surges.

Allowable Subject Matter

4. Claims 5-10 and 17-22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

**The following is an examiner's statement
of reasons for *indicating* Allowable Subject Matter:**

5. Claims 5 and 17 would be allowable because none of the prior art of record disclose a video input protection circuit comprising a first transistor connected in series with a video input terminal between the video input terminal and a termination resistance further comprising a second transistor in combination with the other claim limitations.

Contact information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Boris Benenson whose telephone number is (571) 272-2048. The examiner can normally be reached on M-F (8:20-6:00) First Friday Off.


If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on (571) 272-2800 ext 36. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Boris Benenson
Examiner
Art Unit 2836

B.B.



BRIAN SIRCUS
SUPERVISORY PATENT EXAMINER
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